In the Specification

Please amend the specification as indicated below:

[0006] The FG to CG coupling ratio is determined by: $\alpha_{FC}=C_{FC}/C_{tot}$ where C_{FC} [[if]] is the capacitance between FG 4 and CG 2, and

[0020] A method according to the present invention may furthermore comprise, after forming of the floating gate separator and before forming of the floating gate, reducing the dimensions of the floating gate separator. This way, smaller slits are obtained in an easy way. The dimensions of the floating gate separator may be reduced to sub-lithographic dimensions, whereby dimensions depend on technology node or state of the art and on process conditions. For example for 90 mn generations and beyond, the dimensions of the floating gate separator may reduced to between 100 nm and 40 nm.

[0053] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn [[on]] to scale for illustrative purposes. Where the term "comprising" is used in the present description and claims, it does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun e.g. "a" or "an", "the", this includes a plural of that noun unless something else is specifically stated.

[0055] According to the present invention, in a first step, a substrate 10 or a well in a substrate is provided. In embodiments of the present invention, the term "substrate" may include any underlying material or materials that may be used, or upon which a device, a circuit or an epitaxial layer may be formed. In other alternative embodiments, this "substrate" may include a semiconductor substrate such as e.g. a doped silicon, a gallium arsenide (GaAs), a gallium arsenide phosphide (GaAsP), a germanium (Ge), or a silicon germanium (SiGe) substrate. The "substrate" may include for example, an insulating layer such as a SiO.sub.2 or an Si.sub.3N.sub.4 layer in addition to a semiconductor substrate portion. Thus, the term substrate also includes silicon-on-glass, and silicon-on

sapphire substrates. The term "substrate" is thus used to define generally the elements for layers that underlie a layer or portions of interest. Also, the "substrate" may be any other base on which a layer is formed, for example a glass or metal layer. In the following processing will mainly be described with reference to silicon processing but the skilled person-will appreciate that the present invention may be implemented based on other semiconductor material systems and that the skilled person can select suitable materials as equivalents of the dielectric and conductive materials described below.